

VMS SFRs



The following should be a complete list of the Special Function Registers in the VMS. More detailed descriptions of the registers follow below the list.

Address	Name	Description
100	ACC	Accumulator
101	PSW	Processor Status Word
102	B	B Register (general purpose)
103	C	C Register (general purpose)
104	TRL	Table Reference (Low byte)
105	TRH	Table Reference (High byte)
106	SP	Stack Pointer
107	PCON	Power Control register
108	IE	Interrupt Enable control
109	IP	Interrupt Priority Ranking control
10A-10C		Not Used
10D	EXT	External Memory control
10E	OCR	Oscillation Control Register (32kHz/600kHz/6MHz)
10F		Not Used
110	T0CON	Timer/Counter 0 control
111	T0PRR	Timer 0 Prescaler Data Register
112	T0L	Timer 0 Low
113	T0LR	Timer 0 Low Reload Register
114	T0H	Timer 0 High
115	T0HR	Timer 0 High Reload Register
116-117		Not Used
118	T1CNT	Timer 1 control
119		Not Used
11A	T1LC	Timer 1 Low Compare Data Register
11B	T1L	Timer 1 Low (Read only)
11B	T1LR	Timer 1 Low Reload Register (Write only)
11C	T1HC	Timer 1 High Compare Data Register
11D	T1H	Timer 1 High (Read only)

11D	T1HR	Timer 1 High Reload Register (Write only)
11E-11F		Not Used
120	MCR	Mode Control Register
121		Not Used
122	STAD	Start Addresss Register
123	CNR	Character Number Register
124	TDR	Time Division Register
125	XBNK	Bank Address Register
126		Not Used
127	VCCR	LCD Contrast Control Register
128-12F		Not Used
130	SCON0	SIO0 Control Register
131	SBUF0	SIO0 Buffer
132	SBR	SIO Baud Rate Generator Register
133		Not Used
134	SCON1	SIO1 Control Register
135	SBUF1	SIO1 Buffer
136-143		Not Used
144	P1	Port 1 Latch
145	P1DDR	Port 1 Data Direction Register
146	P1FCR	Port 1 Function Control Register
147-14B		Not Used
14C	P3	Port 3 Latch
14D	P3DDR	Port 3 Data Direction Register
14E	P3INT	Port 3 Interrupt Control Register
14F-15B		Not Used
15C	P7	Port 7 Latch
15D	I01CR	External Interrupt 0, 1 control
15E	I23CR	External Interrupt 2, 3 control
15F	ISL	Input Signal Selection Register
160-162		Not Used
163	VSEL	VMS Control Register
164	VRMAD1	Work RAM Access Address 1
165	VRMAD2	Work RAM Access Address 2
166	VTRBF	Send/Receive Buffer

167	VLREG	Length registration
168-17E		Not Used
17F	BTCR	Base Timer Control Register
180-1FB	XRAM	LCD frame buffer
1FC-1FF		Not Used

PSW - Processor Status Word (101)

7 6 5 4 3 2 1 0
 CY AC - IRBK1 IRBK0 OV RAMBK0 P

CY - Carry flag

The Carry flag is set when a carry from the most significant bit occurs in an addition, or when a borrow to the most significant bit occurs in a subtraction. If an addition or subtraction is performed without a carry or borrow occurring, the Carry flag is cleared.

AC - Auxiliary Carry flag

The Auxiliary Carry flag works like the regular Carry flag, but registers carry from, or borrow to, the third bit.

IRBK - Indirect address register bank

The IRBK bits can be used to set the base address for indirect addressing. See [addressing modes](#) for more information.

OV - Overflow flag

The Overflow flag is set when overflow occurs in a signed addition or subtraction, or when the result of a multiplication exceeds 256. The overflow flag is also set when a division by zero is performed.

RAMBK0 - RAM bank

This bit selects one of two banks for the 256 general purpose RAM bytes at the low half of RAM space (0 through FF). Bank 0 contains system variables and the CPU stack. Bank 1 is free for use by game software, and automatically selected by the VMS firmware before entering game mode.

P - ACC parity

This bit is set when the number of set bits in ACC is odd. Read only.

TRL / TRH - Table Reference register (104 / 105)

The TRL and TRH registers together form a 16-bit (TRL being the low 8 bits and TRH being the high 8 bits) address in ROM space which is used by the LDC instruction. LDC will add the ACC register to this 16-bit address, and fetch the byte at the resulting ROM address back to ACC. The TRL and TRH registers can also be used as general purpose registers.

SP - Stack Pointer (106)

The Stack Pointer points to the topmost element on the stack. The initial value is \$7F, and the stack grows upward from \$80 to \$FF. Note that the stack is always stored in RAM bank 0, regardless of the RAMBK0 setting in PSW.

PCON - Power Control register (107)

This register can be used to suspend the CPU to reduce power consumption. The HOLD and HALT bits will automatically be cleared when execution is resumed.

7 6 5 4 3 2 1 0

- - - - - HOLD HALT

HOLD - Stop CPU and timers

Setting this bit to 1 will put the VMS into deep suspension. The CPU and all timers and clocks will stop.

Only an external interrupt or reset can cause operation to resume.

HALT - Suspend program execution

Setting this bit to 1 will cause the CPU to stop executing instructions. All timers and peripherals will keep operating normally while the CPU is stopped, and any interrupt will wake the CPU up.

IE - Interrupt Enable control (108)

7 6 5 4 3 2 1 0

IE7 - - - - - IE1 IE0

IE7 - Master interrupt enable

When this bit is set to zero, all interrupts will be blocked except nonmaskable ones. (Only the external interrupts INT0 and INT1 can be set to nonmaskable.)

IE1 - INT1 priority level

When this bit is set to one, the priority of external interrupt INT1 is lowered from nonmaskable to low.

IE0 - INT0/INT1 priority level

When this bit is set to one, the priority of both external interrupts INT0 and INT1 are lowered from nonmaskable to low.

OCR - Oscillation Control Register (10E)

The Oscillation Control Register controls the clock frequency of the CPU. Higher frequencies mean increased battery consumption. Subclock mode should be used under normal circumstances.

7 6 5 4 3 2 1 0

OCR7 - OCR5 OCR4 - - OCR1 OCR0

OCR7 - Clock divisor

Setting this bit to zero divides the clock frequency by 12. Setting it to 1 (normal setting) divides the clock frequency by 6.

OCR5 - Subclock mode enable

Setting this bit to one enables subclock mode (32kHz). Subclock mode is significantly slower than normal mode, but is also power conserving and should be used normally to preserve batteries. Setting the bit to zero enables RC clock mode (600kHz).

OCR4 - Main clock mode enable

Setting this bit to one enables the main clock (6MHz). This bit should only be set when subclock mode is disabled, and **only** when docked in the controller.

OCR1 - RC Clock control

Setting this bit to one stops the RC oscillator. This will preserve power, but can naturally only be done in subclock mode.

OCR0 - Main Clock control

Setting this bit to one stops the main clock. This bit should always be set when the VMS is not docked.

T1CNT - Timer 1 control (118)

This register controls the Timer 1 pair of 8-bit timers.

7 6 5 4 3 2 1 0

T1HRUN T1LRUN T1LONG ELDT1C T1HOVF T1HIE T1LOVF T1LIE

T1HRUN - Timer 1 High running

Setting this bit to 1 starts the T1H timer. Setting it to 0 stops the timer.

T1LRUN - Timer 1 Low running

Setting this bit to 1 starts the T1L timer. Setting it to 0 stops the timer.

T1LONG - 16-bit timer enable

Setting this bit to 1 combines T1H and T1L into one 16-bit timer. Setting it to 0 makes T1H and T1L two separate 8-bit timers.

ELDT1C - Timer 1 Compare Data Load Enable

When this bit is set to 0, writes to T1LC and T1HC will not take effect until this bit is set to 1 again.

This can be used to set a 16-bit compare value atomically. (When the timers are not running, this bit is ignored.)

T1HOVF - Timer 1 High Overflow

This bit is set to 1 whenever T1H overflows.

T1HIE - Timer 1 High Interrupt Enable

Setting this bit to 1 enables interrupts (through vector \$2B) when T1H overflows.

T1LOVF - Timer 1 Low Overflow

This bit is set to 1 whenever T1L overflows.

T1LIE - Timer 1 Low Interrupt Enable

Setting this bit to 1 enables interrupts (through vector \$2B) when T1L overflows.

T1LC - Timer 1 Low Compare Data Register (11A)

The T1L timer has a pulse output signal that outputs a 0 when the current timer count is lower than the contents of this register, and a 1 when the current timer count is higher than the contents of this register. The pulse output signal is connected to the VMS beeper, which makes it possible to use this feature to play a square sound wave.

T1L / T1LR - Timer 1 Low (Reload) Register (11B)

The T1L and T1LR registers occupy the same address in the SFR area. When the address is read, you get the value of T1L. When it is written, the data is stored into T1LR. T1L is the current Timer 1 Low count, and is automatically incremented 32768/6 times per second when the timer is running. When it reaches 256, an overflow is detected (optionally generating an interrupt, see [T1CNT](#)), and the counter is reloaded from the T1LR register. The period of the timer is thus $(256 - T1LR) / (32768 / 6)$ seconds.

MCR - Mode Control Register (120)

This register controls the operation mode of the LCD.

7 6 5 4 3 2 1 0

? ? ? MCR4 MCR3 - - MCR0

MCR4 - Refresh rate

Setting this bit to 1 gives a display refresh rate of 166Hz. Setting it to 0 gives a rate of 83Hz.

MCR3 - Refresh control

Setting this bit to 0 stops refreshing the LCD.

MCR0 - Graphics mode

Setting this bit to 1 selects graphics mode.

VCCR - LCD Contrast Control Register (127)

7 6 5 4 3 2 1 0

VCCR7 ? - - - - -

VCCR7 - LCD display enable

Set this bit to 1 to enable LCD display. Always make sure to enable LCD refresh before setting this bit. Also, always clear this bit before disabling LCD refresh.

P1 - Port 1 Latch (144)

Port 1 is connected to the external connector on the VMS unit.

7 6 5 4 3 2 1 0

- - pin 12 pin 10 pin 11 pin 3 pin 4 pin 5

P3 - Port 3 Latch (14C)

Port 3 is connected to the keys on the VMS unit. A 0 means key pressed, a 1 means key not pressed.

7 6 5 4 3 2 1 0

SLEEP MODE B A

P3INT - Port 3 Interrupt Control Register (14E)

Interrupts can be generated when the keys on the VMS unit are pressed. They are controlled with this register.

7 6 5 4 3 2 1 0

- - - - - P32INT P31INT P30INT

P32INT - Port 3 interrupt control

Set this bit to 1 to allow P3 input to break HOLD mode (see [PCON](#))

P31INT - Port 3 interrupt flag

This bit is set to 1 when there is input on P3. It must be cleared manually by the interrupt service handler.

P30INT - Port 3 interrupt enable

Set this bit to 1 to enable interrupts to occur when P31INT is set.

P7 - Port 7 Latch (15C)

This is an input-only port.

7 6 5 4 3 2 1 0

- - - - P73 P72 P71 P70

P73 - External connector pin 6

This bit reflects the state of pin 6 on the external connector.

P72 - External connector pin 13

This bit reflects the state of pin 13 on the external connector.

P71 - Battery voltage

This bit turns to a zero when battery power starts running low. It is monitored by the system time update interrupt, unless disabled with system variable 06E.

P70 - External voltage

This bit turns to a one when there is external 5V voltage available. This happens when the VMS is inserted into a controller plugged into a Dreamcast with the power on.

VSEL - VMS Control Register (183)

7 6 5 4 3 2 1 0

- - - INCE - - ? ?

INCE - VRMAD Auto Increment

If this bit is set, the VRMAD1/VRMAD2 register is automatically incremented after a load or store to VTRBF.

VRMAD - Work RAM Access Address (164,165)

This 9 bit register holds the address of the Work RAM location that can be accessed through VTRBF. VRMAD1 (\$164) holds the 8 least significant bits, VRMAD2 (\$165) holds the most significant bit.

VTRBF - Send/Receive Buffer (186)

This register provides access to the 256 byte Work RAM area. Reading from this register will read a byte from the Work RAM, and writing to this register will write a byte to the Work RAM. The Work RAM address accessed is determined by the contents of the VRMAD1 register. The address can optionally be auto-incremented, see [VSEL](#).

XRAM - LCD frame buffer (180 - 1FB)

The LCD frame buffer is divided into three banks, selected using the XBNK register. The upper half of the dot matrix display is contained in bank 0, and the lower half in bank 1. The four icons at the bottom of the display is controlled with bank 2.

The organization of each dot matrix bank is as follows: Each 48 pixel line is stored as six bytes, the first one being the eight leftmost pixels and so on. Within each byte, the most significant bit is leftmost. The data for each pair of two lines is stored consecutively, but then there is a brief skip of four in the address space before the next two lines. The organization of bank 0 is shown below. For bank 1, just add 16 to the line numbers.

0-7 8-15 16-23 24-31 32-39 40-47

0	180	181	182	183	184	185
1	186	187	188	189	18A	18B
2	190	191	192	193	194	195
3	196	197	198	199	19A	19B
4	1A0	1A1	1A2	1A3	1A4	1A5

5	1A6	1A7	1A8	1A9	1AA	1AB
6	1B0	1B1	1B2	1B3	1B4	1B5
7	1B6	1B7	1B8	1B9	1BA	1BB
8	1C0	1C1	1C2	1C3	1C4	1C5
9	1C6	1C7	1C8	1C9	1CA	1CB
10	1D0	1D1	1D2	1D3	1D4	1D5
11	1D6	1D7	1D8	1D9	1DA	1DB
12	1E0	1E1	1E2	1E3	1E4	1E5
13	1E6	1E7	1E8	1E9	1EA	1EB
14	1F0	1F1	1F2	1F3	1F4	1F5
15	1F6	1F7	1F8	1F9	1FA	1FB

Organization of bank 2:

	7	6	5	4	3	2	1	0
181	-	file icon	-	-	-	-	-	-
182	-	-	-	game icon	-	-	-	-
183	-	-	-	-	-	clock icon	-	-
184	-	-	-	-	-	-	-	flash access icon

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